System Validation and Verification (Systems Engineering)

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Historically, the terms validation and verification have been very loosely defined in the system engineering world, with predictable confusion. Few hardware or software testing texts even touch upon validation and verification, despite the fact that, properly employed, these test tools offer system and test engineers powerful techniques for identifying and solving problems early in the design process. Together, validation and verification encompass testing, analysis, demonstration, and examination methods used to determine whether a proposed design will satisfy system requirements.

System Validation and Verification clear definitions of the terms and detailed information on using these fundamental tools for problem solving. It smoothes the transition between requirements and design by providing methods for evaluating the ability of a given approach to satisfy demanding technical requirements. With this book, system and test engineers and project managers gain confidence in their designs and lessen the likelihood of serious problems cropping up late in the program. In addition to explanations of the theories behind the concepts, the book includes practical methods for each step of the process, examples from the author's considerable experience, and illustrations and tables to support the ideas.

Although not primarily a textbook, System Validation and Verification is based in part on validation and verification courses taught by the author and is an excellent supplemental reference for engineering students. In addition to its usefulness to system engineers, the book will be valuable to a wider audience including manufacturing, design, software , and risk management project engineers - anyone involved in large systems design projects.

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